IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (previously presented) A method, comprising:

identifying a combination of fields in a header of an internet protocol (hereinafter IP) packet, wherein the combination is dynamically modifiable; and

utilizing the combination of fields to classify the IP packet.

2. (previously presented) The method according to claim 1, further comprising:

a. constructing a key according to information in a key construction register;

b. identifying a tag that corresponds to the key from a table of key-tag entries in a memory device; and

c. inserting the tag in the header of IP packet in accordance to information in a tag insertion register.

3. (previously presented) The method according to claim 2, wherein the information in the key construction register indicates a retrieval location in the header of IP packet and a number of bits from the retrieval location to consider in constructing the key.

4. (previously presented) The method according to claim 2, wherein the information in the tag insertion register indicates a number of bits to retrieve from the tag and an insertion location in the header of IP packet to insert the tag.

5. (previously presented) A broadband engine, comprising:

a. a transceiver module; and

b. a lookup module, coupled to an external processor via an external processor interface, an external content adjustable memory and the transceiver module, further including:

a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet.

6. (original) The broadband engine according to claim 5, the transceiver module further

a. collects a portion of incoming packets; and

b. appends control information to the collected portion.

7. (previously presented) The broadband engine according to claim 5, the lookup module further comprising:

a. a plurality of registers to contain key construction information and tag insertion information from the external processor; and

b. the processing core to construct a key according to the key construction information, retrieve a tag that corresponds to the key from the external content adjustable memory and insert the tag in a header of one of the packets based on the tag insertion information.

8. (previously presented) The broadband engine according to claim 7, wherein the key construction information further comprises:
a retrieval location in the header of IP packet and a number of bits from the retrieval location to consider in constructing the key.

9. (previously presented) The broadband engine according to claim 7, wherein the tag insertion information further comprises:
a number of bits to retrieve from the tag and an insertion location in the header of IP packet to insert the tag.

10. (previously presented) A line card, comprising:
an input/output interface;
a switch fabric interface to communicate with a switch fabric; and

a broadband engine, coupled to the input/output interface and the switch fabric interface, further including:

a. a transceiver module to receive a plurality of packets from the input/output interface; and

b. a lookup module, coupled to an external content adjustable memory, the transceiver module and an external processor, further including:

a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet.

11. (original) The line card according to claim 10, the transceiver module further

a. collects a portion of incoming packets; and

b. appends control information to the collected portion.

12. (previously presented) The line card according to claim 10, the lookup module further comprising:

a. a plurality of registers to contain key construction information and tag insertion information from the external processor; and

b. the processing core to construct a key according to the key construction information, retrieve a tag that corresponds to the key from the

external content adjustable memory and insert the tag in a header of one of the packets based on the tag insertion information.

13. (previously presented) The line card according to claim 12, wherein the key construction information further comprises:
a retrieval location in the header of IP packet and a number of bits from the retrieval location to consider in constructing the key.

14. (previously presented) The line card according to claim 12, wherein the tag insertion information further comprises:
a number of bits to retrieve from the tag and an insertion location in the header of IP packet to insert the tag.

15. (previously presented) A communication system, comprising:

a. a switch fabric;

b. a main processing engine with an processor; and

c. a line card, coupled to the switch fabric via a switch fabric interface, further including:

an input/output interface;

a broadband engine, coupled to the input/output interface and the switch fabric interface, further comprising:

i. a transceiver module to receive a plurality of packets from the input/output interface; and

ii. a lookup module, coupled to an external content adjustable memory, the transceiver module and the processor, further including:
a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet.

16. (original) The communication system according to claim 15, the transceiver module further

a. collects a portion of incoming packets; and

b. appends control information to the collected portion.

17. (previously presented) The communication system according to claim 15, the lookup module further comprising:

a. a plurality of registers to contain key construction information and tag insertion information from an external central processing unit; and

b. the processing core to construct a key according to the key construction information, retrieve a tag that corresponds to the key from the external content adjustable memory and insert the tag in a header of one of the packets based on the tag insertion information.

18. (previously presented) The communication system according to claim 17, wherein the key construction information further comprises:

a retrieval location in the header of IP packet and a number of bits from the retrieval location to consider in constructing the key.

19. (previously presented) The communication system according to claim 17, wherein the tag insertion information further comprises:
a number of bits to retrieve from the tag and an insertion location in the header of IP packet to insert the tag.

COMMENTS

The enclosed is responsive to the Examiner's Final Office Action mailed on September 24, 2004 and is being filed pursuant to a Request for Continued Examination (RCE) as provided under 37 CFR 1.114. At the time the Examiner mailed the Office Action claims 1-19 were pending. By way of the present response the Applicants have: 1) amended no claims; 2) added no claims; and 3) cancelled no claims. As such, claims 1-19 are now pending. The Applicants respectfully request reconsideration of the present application and the allowance of all claims.

Claim Objections

The proper Status Identifiers have been included in this office action response.

Claim Rejections

35 U.S.C. 102(e) Rejections

The Examiner rejected claims 1-5, 7-10, 12-15 and 17-19 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,275,861, Chaudri, et al. (hereinafter "Chaudri").

Claim 1 states:

> 1. A method, comprising:
> identifying a combination of fields in a header of an internet protocol (hereinafter IP) packet, wherein the combination is dynamically modifiable; and
> utilizing the combination of fields to classify the IP packet.
> (Emphasis added)

In regards to claim 1, the Examiner states the phrase, "wherein the combination is dynamically modifiable" is met by Chaudri (page 2-3 of the office action mailed 9/24/04). Applicants respectfully disagree that Chaudri discloses this limitation of claim 1. Chaudri does not disclose, "wherein the combination is dynamically modifiable." In contrast, Chaudri merely discloses that a search engine comprises registers that are alterable parameters of the search engine itself. Chaudri discloses:

> In this embodiment is depicted search engine 110 including registers or similar memory locations for flow identification 117a, mask 117b, offset 117c, extracted packet data 110a, and search key 116. According to one embodiment of the invention, these registers are the alterable parameters of search engine 104 which will otherwise perform its search function using fast dedicated custom logic circuits. These alterable registers may be set up to default values by a management program. According to the invention, search engine 104 is able to very quickly derive a search key from a data packet according to the values specified in the registers 117b and 117c. This search key is then used to look up a data structure for a next flow identification and this data structure is used to derive new values for flow id 117a, mask 117b, and offset 117c.
>
> (Emphasis Added)
> (Col. 6, lines 39-49)

A search engine comprising alterable registers is not the same as the combination is dynamically modifiable.

Further, the Examiner states:

> Based on this interpretation, the examiner asserts the use of 'alterable registers' (also referred to as 'parameters') as taught by Chaudri would be within the scope of the limitations regarding the dynamic modification of a combination of header fields.
>
> (Page 10 of the office action mailed 09/24/04).

Applicants respectfully disagree. Alterable parameters as taught by Chaudri merely refer to alterable parameters of a search engine so that a search routine may be

customized. This is further supported in the abstract of Chaudri, which states, "Flexibility is achieved by allowing parameters of the search routine to be specified in memory which can be programmably altered." (Emphasis added). Therefore Chaudri fails to disclose each and every element of claim 1. Hence, Chaudri does not anticipate claim 1 under 35 U.S.C. §102(e).

Claims 2-4 depend on and include the limitations of claim 1. Therefore, Chaudri also fails to anticipate claims 2-4 under 35 U.S.C. §102(e).

Claim 5 states:

> 5. A broadband engine, comprising:
> a transceiver module; and
> a lookup module, coupled to an external processor via an external processor interface, an external content adjustable memory and the transceiver module, further including:
> a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet.
> (Emphasis added)

In regards to independent claim 5, the Examiner states the phrase, "a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet" is met by Chaudri (page 3-4 of the office action mailed 9/24/04). Applicants respectfully disagree that Chaudri discloses this limitation of claim 5. Chaudri does not disclose "a dynamically modifiable combination of fields in a header of the IP packet" for the same reason as mentioned above in regards to claim 1. As stated above, Chaudri merely discloses that a search engine comprises registers that are alterable parameters of the search engine itself. Therefore Chaudri fails to disclose each and every element of claim 5. Hence, Chaudri does not anticipate claim 5 under 35 U.S.C. §102(e).

Claims 6-9 depend on and include the limitations of claim 5. Therefore, Chaudri also fails to anticipate claims 6-9 under 35 U.S.C. §102(e).

Claim 10 states:

> 10. A line card, comprising:
> an input/output interface;
> a switch fabric interface to communicate with a switch fabric; and
> a broadband engine, coupled to the input/output interface and the switch fabric interface, further including:
> a transceiver module to receive a plurality of packets from the input/output interface; and
> a lookup module, coupled to an external content adjustable memory, the transceiver module and an external processor, further including:
> a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet.

(Emphasis added).

In regards to independent claim 10, the Examiner states the phrase, "a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet" is met by Chaudri (page 5 of the office action mailed 9/24/04). Applicants respectfully disagree that Chaudri discloses this limitation of claim 10. Chaudri does not disclose "a dynamically modifiable combination of fields in a header of the IP packet" for the same reason as mentioned above in regards to claim 1. As stated above, Chaudri merely discloses that a search engine comprises registers that are alterable parameters of the search engine itself. Therefore Chaudri fails to disclose each and every element of claim 10. Hence, Chaudri does not anticipate claim 10 under 35 U.S.C. §102(e).

Claims 11-14 depend on and include the limitations of claim 10. Therefore, Chaudri also fails to anticipate claims 11-14 under 35 U.S.C. §102(e).

Claim 15 states:

> 15. A communication system, comprising:
> a switch fabric;
> a main processing engine with an processor; and
> a line card, coupled to the switch fabric via a switch fabric interface, further including:
> an input/output interface;
> a broadband engine, coupled to the input/output interface and the switch fabric interface, further comprising:
> a transceiver module to receive a plurality of packets from the input/output interface; and
> a lookup module, coupled to an external content adjustable memory, the transceiver module and the processor, further including:
> a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet.

(Emphasis added).

In regards to independent claim 15, the Examiner states the phrase, "a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet" is met by Chaudri (page 6 of the office action mailed 9/24/04). Applicants respectfully disagree that Chaudri discloses this limitation of claim 15. Chaudri does not disclose "a dynamically modifiable combination of fields in a header of the IP packet" for the same reason as mentioned above in regards to claim 1. As stated above, Chaudri merely discloses that a search engine comprises registers that are alterable parameters of the search engine itself. Therefore Chaudri fails to disclose each and every element of claim 15. Hence, Chaudri does not anticipate claim 15 under 35 U.S.C. §102(e).

Claims 16-19 depend on and include the limitations of claim 15. Therefore, Chaudri also fails to anticipate claims 16-19 under 35 U.S.C. §102(e).

35 U.S.C. 103(a) Rejections

The Examiner rejected claims 6, 11 and 16 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,275,861, Chaudri, et al. (hereinafter "Chaudri") in view of U.S. Patent 6,611,875, Chopra, et al. (hereinafter "Chopra").

Dependent claims 6, 11 and 16 depend upon and include the limitations of independent claims 5, 10 and 15, respectively. As stated above, Chaudri does not teach or suggest, "a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet." Further, Chopra does not teach or suggest, "a processing core to classify an internet protocol (hereinafter IP) packet by utilizing a dynamically modifiable combination of fields in a header of the IP packet." In contrast, Chopra is completely silent on the limitation. Therefore, the combination of Chaudri and Chopra fail to make claims 6, 11 and 16 obvious under 35 U.S.C. §103(a).

In light of the comments above, the Applicants respectfully request the allowance of all claims.

Comments

If there are any additional charges, please charge Deposit Account No. 02-2666. If a telephone interview would in any way expedite the prosecution of this application, the Examiner is invited to contact Michael J. Mallie at (408) 720-8300.

Respectfully submitted,

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